Michael Kellett
Electronics and Software Consultant

Behavioural model of ADS8320 A-D converter in VHDL

Introduction

The Burr Brown ADS8320 is a low cost, low power 16 bit A-D converter. This VHDL behavioural model was written to allow testing of an FPGA design which interfaced the converter with a processor and memory on the digital side and a multiplexor on the analogue side.

To understand the model you will need to download the Burr Brown data sheet which is available on their web site at analog.ti.com

Model

The model is based on the behavior of the ADS8320 as described in the data sheet dated December 1998.

Inputs and Outputs

There are three inputs, DCLOCK and CS which are present on the chip and AN_DATA which is a 16 bit vector used to set the ‘analogue’ signal.

There is one output, DATA.

All inputs and outputs are STD_LOGIC or STD_LOGIC_VECTOR.

Internal signals and variables

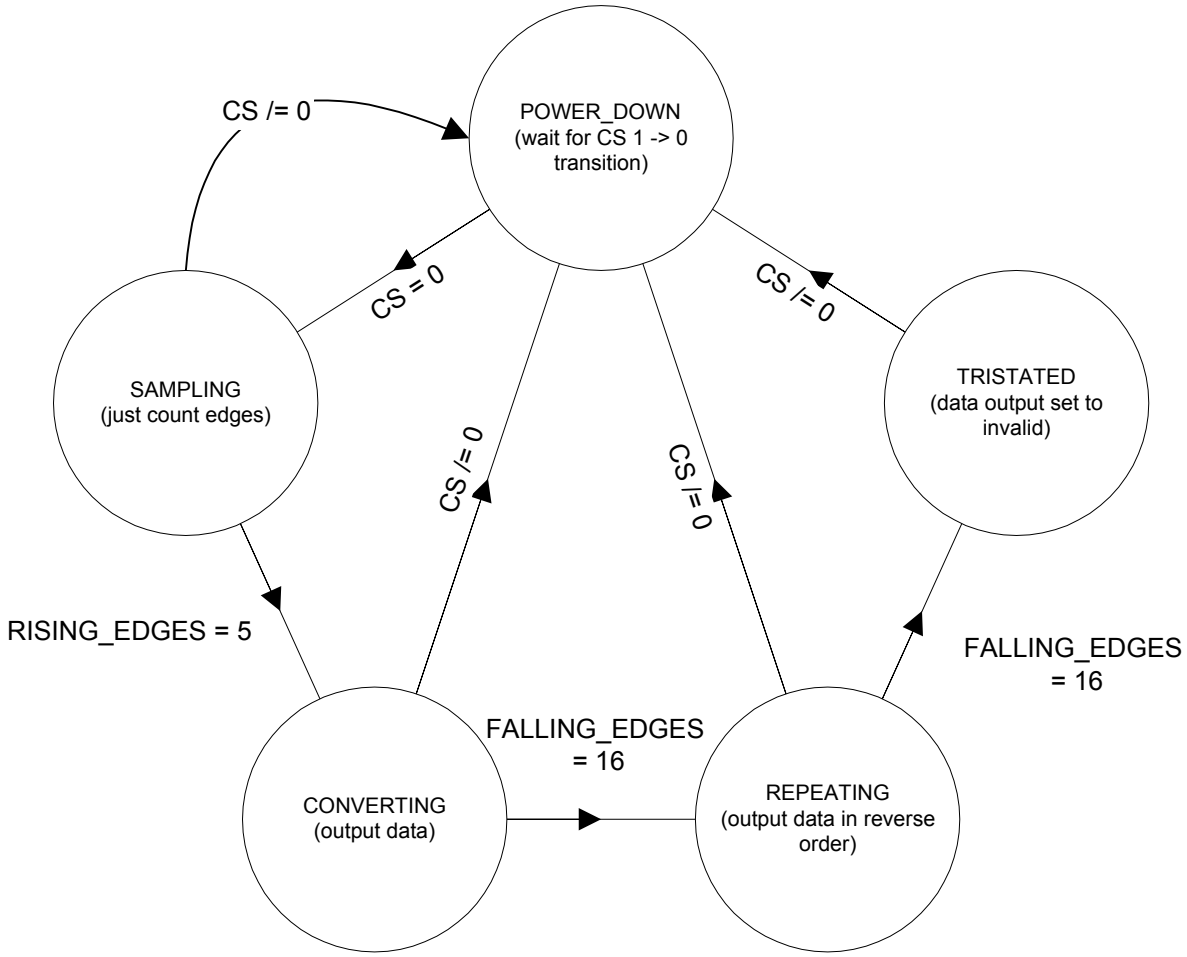
Four variables are used internally:

STATE	a user type to track the state machine
RISING_EDGES	integer used to count rising edges on DCLOCK
FALLING_EDGES	integer used to count falling edges on DCLOCK
CURRENT_BIT	pointer to and counter of ‘analogue’ bit to output

Modelling Strategy

The ADS8320 is represented by a 5 state FSM. CS = 1 is treated as an asynchronous reset to the POWER_DOWN state. CS -> 0 causes a transition from the POWER_DOWN to the SAMPLING state.

This is not strictly accurate since the actual chip prohibits CS -> 0 within 20nS of DCLOCK -> 1. The model merely requires this setup time to be greater than zero so any use of the model must check for illegal transitions of CS to close to DCLOCK -> 1.



VHDL

A correctly formatted listing of the VHDL code is contained in b8320.pdf. The code was written and tested with Aldec Active-HDL which also produced the listing. I could find no simple way of preserving the formatting if the listing was imported into Word.

Summary

This is a simple behavioural model of the Burr Brown ADS8320 A-D converter and is intended to facilitate construction of a VHDL test bench for projects interfacing with that chip.

If you would like to discuss this model or any other data acquisition or embedded system related problem please contact me.

Michael Kellett,

Electronics and Software Consultant.

mk@mkesc.co.uk